❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title : **French for foreigners**	
Module leader: Nathalie CARADEC (nathalie.caradec@enssat.fr)	
Type of module: Compulsory module Prerequisite: placement test for level group	
Duration of module : 30h	
Module components /Types of Courses • Practical courses in small group Dialogues- role play –variety of teaching material through the media and digital technology	
ECTS: 4	
Work load: -In class studying: 30h -Student managed learning: 20h	
Content: CEFR French levels are used on the four skills speaking – listening-reading and writing • Level A1-A2 can introduce him/herself, can ask and answer questions about personal details such as where he/she lives, people he/ she knows, and things he/she has. Can interact in a simple way provided the other person talks slowly and clearly. • Level B1-B2 Can understand the main points of clear standard input on familiar matters regularly encountered in work, school, leisure, etc. Can deal with most situations likely to arise whilst travelling in an area where the language is spoken. Can produce simple connected text on topics which are familiar or of personal interest. Can describe experiences and events, dreams, hopes & ambitions and briefly give reasons and explanations for opinions and plans. Common European Framework of References : CECRL (Cadre Européen Commun de Références pour les Langues)	
Learning outcomes: Development of the different skills according to the level.	
Assessment - Written assignment - Oral assignment	
Language of instruction: French	
Additional information	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title:	**Integrated systems and high-level synthesis**
Module leader:	Emmanuel CASSEAU (emmanuel.casseau@enssat.fr)
Type of module (compulsory module, required Elective module, elective module)	Compulsory module
Duration of module	24 hours
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	Lecture : 18 h, lab : 6 h
ECTS: 2	
Work load	-In class studying: 24h -Student managed learning: 18h

Content

- Hardware technologies and applications
- System on Chip (SoC): architectural solutions, hardware platforms
- Design flow and SoC design methodologies
- Signal flow graph, algorithmic transformations (retiming, pipelining, parallelization, associativity, distributivity)
- Principle of high level synthesis
- High level synthesis steps (scheduling, allocation, binding, optimizations) and associated techniques

Learning outcomes

At first, this course aims to present what is a system-on-a-chip (SoC) and the principles of SoC design. The methodologies as well as the main used tools are presented. Then the goal is to present a method for designing specific digital circuits aimed at automating the transition from a high-level description of an application to its hardware description while allowing to explore the design space (mainly throughput versus area). This method is called high level synthesis. The targeted applications are signal processing-based ones. Typically, the application is represented in the form of a signal flow graph on which formal transformations will be applied in order to optimize its hardware implementation according to certain criteria (surface, flow, etc.). The various steps and techniques (transformations, component selection, scheduling, binding) of the high-level synthesis process are detailed.

Assessment

- Written assignment ☑

Language of instruction	ENGLISH
Additional information: B1 level is a prerequisite	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title	**System on Chip Conception**
Module leader	Bertrand LE GAL (Bertrand.le-gal@enssat.fr)
Type of module (compulsory module, required Elective module, elective module)	Compulsory module
Duration of module	18 hours
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	Lectures (6h) and Lab (12h)
ECTS: 2	
Work load	-In class studying: 18 hours -Student managed learning : 18 hours

Content

This lecture presents the key aspect associated to System On Chip (SoC) design. SoC are platforms that embedded a processor and hardware accelerator, jointly with inputs/outputs and dedicated co-processors. SoC are now massively used in industry (phones, hardware platforms, and many devices…) and cannot be reduced to the simple concatenation of general-purpose processor (GPP) and hardware accelerators. It is necessary to propose new design flow that considers the advantages of these platforms.

Besides that, as the space design is wide (both in hardware and software) it is necessary to optimally distribute the process in the hardware part and the software part: this is called the Hardware/software (HW/SW) partitioning and is matter of importance to benefit from the SoC special architecture.

Finally, an introduction on embedded Linux and how to map hardware accelerator at the operating system level is presented.

In the labs, the students will use a Zybo board with Vivado in order to create a signal processing application and see the performance difference between a pure software approach and a HW/SW approach

Learning outcomes

- SoC architectures and specificities
- SoC design flow
- Hardware/software partitioning
- Embedded Linux
- Vivado tools and Zybo board.

Assessment

- Oral assignment ☑

Language of instruction

ENGLISH

Additional information: B1 level is a prerequisite

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title:	**High Performance Processor**
Module leader:	Daniel CHILLET (daniel.chillet@enssat.fr)
Type of module: (compulsory module, required Elective module, elective module)	Compulsory module
Duration of module: 20 hours	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	Lecture (22 h), exercise (4 h) and labs (8 h)
ECTS: 3	
Work load	-In class studying: 34 h -Student managed learning: 26 h
Content • Introduction • Reminders on basic computer architecture (pipeline, cache memory) • Advanced techniques for high performance processors • Graphical Processing Unit architecture and programming	
Learning outcomes The aim of this courses is to explain how the processors have evolved since the first model, also called Von Neumann processor. The course discusses why and how these processors deliver high performance computing capability and which techniques are implemented in these processors to provide more and more performance, year by year. Several techniques are highlighted and explained with several examples. The last part of the course is about GPU architecture and programming. From this course, the students will be able to understand how recent processors work and they will also be able to optimize their code in order to exploit the processors performances.	
Assessment - Written assignment ☑ - Oral assignment ☑	○ Coefficient **2**
Language of instruction	ENGLISH
Additional information: B1 level is a prerequisite	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title **Code compilation and Optimisation**	
Module leader Bertrand LE GAL (Bertrand.le-gal@enssat.fr)	
Type of module (compulsory module, required Elective module, elective module) Compulsory module	
Duration of module 16 hours	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …) Lectures (6h) and Lab (10h)	
ECTS: 1	
Work load -In class studying: 16 hours -Student managed learning: 12 hours	
Content This course provides the foundational understanding of the mechanisms behind code compilation and optimization, with the goal of producing efficient application implementations on modern processor architectures. **Compilation Flow** • Organization of the GCC Compilation Flow • Makefile Tool • Program Execution **Code Performance Measurement** • Instrumentation: Invasive/Non-invasive Profiling • Some Tools: gprof, valgrind **Code Optimization** • Role of Optimizations in the Compilation Flow • Optimization with GCC • Optimization in Relation to Memory Hierarchy	
Learning outcomes The objective of this course is to understand and master the stages of compiling code written in the C language, to measure a program's performance, and to identify bottlenecks. At the end of the course, students will be able to understand the compilation and code optimization techniques available in modern compilers, with the aim of producing implementations that are efficient in terms of both execution time and energy consumption. The major categories of code optimization will be studied, particularly those that take into account memory hierarchy. Execution analyses will enable students to link processor architectures with their impact on code execution.	
Assessment - Written assignment ☑	
Language of instruction ENGLISH	
Additional information: B1 level is a prerequisite	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title **Optimization and artificial intelligence technics**	
Module leader Pascal SCALART (pascal.scalart@enssat.fr)	
Type of module (compulsory module, required Elective module, elective module) Elective module	
Duration of module 34 hrs	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …) lectures (24 hrs), tutorial 6 hours and lab (4 hrs)	
4 ECTS	
Work load -In class studying: 34 hrs -Student managed learning: 42 hrs	
Content **Pixel Classification in Hyperspectral Imaging:** The objective is to implement and compare several sequential approaches for dimensionality reduction (PCA, ICA, autoencoder) and supervised classification (k-NN, LDA, SVM, MLP, and other neural network-based approaches) for pixel classification with partial knowledge of the class membership of a training sample.	
Learning outcomes At the end of the course, the student can • **Implement signal and image processing tools and domain-specific applications** • **Apply reasoning, methods, and mathematical tools** • **Analyze and formalize a problem**	
Assessment - Written assignment ☑	
Language of instruction FRENCH or ENGLISH	
Additional information: B1 level is a prerequisite.	

ENSSAT LANNION | Université de Rennes

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title **Project: artificial intelligence (design and simulation)**	
Module leader Pascal SCALART (pascal.scalart@enssat.fr)	
Type of module (compulsory module, required Elective module, elective module) Elective module	
Duration of module 22 hrs	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …) lab (22 hrs)	
2 ECTS	
Work load -In class studying 22 hrs -Student managed learning 32 hrs	
Content This course focuses on the practical implementation of artificial intelligence techniques for solving classification or segmentation tasks using neural networks. Students will design and train a neural network in Python, applying tools such as PyTorch. The course also emphasizes the analysis of project requirements and performance evaluation, guiding students through the entire process from understanding the problem to building a solution and measuring its success. This module is followed by **artificial intelligence (implementation)** where the designed solution is implemented on a hardware target.	
Learning outcomes • Understand and apply AI methodologies for classification and segmentation tasks. • Design, train, and evaluate neural networks using Python and machine learning frameworks. • Analyze a project's specifications and translate them into an appropriate AI solution. • Measure and interpret performance metrics to assess the effectiveness of the model.	
Assessment - Written assignment ☑	
Language of instruction FRENCH or ENGLISH	
Additional information: B1 level is a prerequisite.	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title	**Project: artificial intelligence (Implementation)**
Module leader	Bertrand LE GAL (Bertrand.le-gal@enssat.fr)
Type of module (compulsory module, required Elective module, elective module)	Elective module
Duration of module	10 hrs
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	lab (10 hrs)
2 ECTS	
Work load	-In class studying 10 hrs -Student managed learning 24 hrs
Content This course is designed to guide students through the process of deploying AI models, specifically neural networks, on hardware equipped with GPUs for enhanced performance. Building on previous work in neural network design and training, students will focus on optimizing and implementing their AI solutions on hardware platforms with NVIDIA GPUs. The course covers GPU programming, model optimization for hardware acceleration, and performance measurement in real-world settings.	
Learning outcomes • Implement and deploy neural networks on GPU hardware for classification/segmentation tasks. • Optimize AI models for GPU-based hardware to improve training speed and inference efficiency. • Measure and analyze the performance of AI solutions on hardware platforms.	
Assessment - Written assignment ☑	
Language of instruction	FRENCH or ENGLISH
Additional information: B1 level is a prerequisite. Modules **artificial intelligence (design and simulation)** and **High Performance Processor** are prerequisite.	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title **Source Coding**	
Module leader Pascal SCALART (pascal.scalart@enssat.fr)	
Type of module (compulsory module, required Elective module, elective module) Elective module	
Duration of module 16 hrs	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …) lectures (8 hrs) and lab (8 hrs)	
1 ECTS	
Work load -In class studying: 16 hrs -Student managed learning: 12 hrs	
Content Source coding aims at compressing data (analog or digital) to provide an efficient binary representation of these data (i.e. a high compression ratio) while preserving the essential information they convey (i.e. a low distortion). Source coding are used to transmit or store data such as speech, image or video data, and is strongly related to other specific applications such as image classification, speech recognition, face recognition, etc.	
Learning outcomes At the end of the course, the student can • Identify the different families of audio/speech and image/video codecs; • Analyze and characterize the performances of several quantization techniques: scalar quantization (uniform and non-uniform), vector quantization; • Understand the properties of the main audio codecs for use in fixed (xDSL, DVB) and mobile (GSM, 3G, 4G/LTE) networks; • Understand the basis of perceptual audio coding: psychoacoustics and quantization noise shaping; • Identify the main functions embedded in a H.264-like codec (inter- and intra-frame prediction; motion estimation/compensation; analysis-by-synthesis codecs).	
Assessment - Written assignment (Lab report) ☑	
Language of instruction FRENCH or ENGLISH	
Additional information: B1 level is a prerequisite	

ENSSAT LANNION | Université de Rennes

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title	**Wireless communications**
Module leader	Robin GERZAGUET (robin.gerzaguet@enssat.fr)
Type of module (compulsory module, required Elective module, elective module)	Compulsory module
Duration of module 30 hours	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	Lectures (20h) and Lab (10h)
3 ECTS	
Work load	-In class studying 30 hours -Student managed learning 28 hrs

Content

This lecture presents the constraints and specificities of wireless transmissions. Several key physical aspects are presented such as digital baseband model of carrier frequency transmissions and deterministic and probabilistic multipath channel models.
The second part of the lecture is dedicated to signal processing techniques dedicated to wireless transmissions and focus on the physical layer: the mathematical model of Orthogonal Frequency Division Multiplexing (OFDM) is presented jointly with the core aspect of the waveform. Several standards based on OFDM are finally introduced (WiFi, LTE-4G, expected 5G…)
In the lab, the student will implement an 5G-NR receiver in Python

Learning outcomes

- Digital baseband model
- Multipath channel model (WSS)
- Rayleigh and Rice channel model
- Orthogonal Frequency Division Multiplexing (OFDM)
- WiFi and 5GNR standards

Assessment

- Oral assignment ☑

Language of instruction

ENGLISH

Additional information: B1 level is a prerequisite

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title	**Hardware Security**
Module leader	Robin GERZAGUET (robin.gerzaguet@enssat.fr)
Type of module (compulsory module, required Elective module, elective module)	Compulsory module
Duration of module	16 hours
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …)	Lectures (13h) and Lab (12h)
2 ECTS	
Work load	-In class studying 25 hours -Student managed learning 20 hrs
Content	This course provides an in-depth understanding of hardware and software security aspects using Software Defined Radio (SDR) technology. Students will explore various attack vectors, countermeasures, and practical techniques for securing hardware and software systems. The course includes both theoretical lectures and hands-on laboratory sessions where students will gain practical experience in real-time eavesdropping and algorithm design using SDR. Part 1: Definitions, Taxonomy, and Attackers Part 2: Hardware Attacks Part 3: Emanation Attacks Part 4: Software Defined Radio (SDR) Part 5: Countermeasures Lab : Real-time eavesdropping of screens using SDR - Setting up SDR hardware and software - Capturing and analyzing electromagnetic emanations - Designing algorithms for screen eavesdropping
Learning outcomes	- Hardware security asset especially electro-magnetic ones - Models and exploits of EM side channel - Use of SDR and associated digital signal processing techniques - Processor vulnerabilities and countermeasures
Assessment	- Written assignment (Lab report) ☑
Language of instruction	ENGLISH
Additional information: B1 level is a prerequisite	

❒1st / ❒2nd/☑ 3rd year /☑ Winter /❑ Spring semester

Module title **Technical project**	
Module leader Robin GERZAGUET (robin.gerzaguet@enssat.fr)	
Type of module (compulsory module, required Elective module, elective module) Compulsory module	
Duration of module 60 hours	
Module components /Types of Courses (lectures, practical course, lab, tutorial, internship, …) Lab (60h)	
10 ECTS	
Work load -In class studying 60 hours -Student managed learning 180 hrs	
Content This course offers students the opportunity to engage in a hands-on engineering project linked to current research topics in digital technologies, embedded systems, or artificial intelligence (AI). The project will emphasize interdisciplinary collaboration, research-driven problem-solving, and the application of advanced engineering principles. Students will work on real-world challenges, developing solutions that could be implemented in ongoing research or industrial applications.	
Learning outcomes - Apply advanced digital, embedded systems, or AI techniques to solve research or industry-related challenges. - Design, develop, and implement innovative engineering solutions based on real-world requirements. - Understand the interplay between research and engineering development. - Present and document technical solutions in line with research and industry standards.	
Assessment - Written assignment ☑ - Oral assignment ☑	
Language of instruction ENGLISH	
Additional information: B1 level is a prerequisite	